```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 19
description:
top level BOM
----------------------------
revision 3.887
date: 1995/06/30 02:54:34;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

latest top level placement/timing files.  950/1000
----------------------------
revision 3.886
date: 1995/06/30 00:26:59;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/doc
      testerinit.html

Initial release
----------------------------
revision 3.885
date: 1995/06/29 18:49:06;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/doc
      verify.html

add description for command_test_addr to verify.html
----------------------------
revision 3.884
date: 1995/06/29 18:40:24;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

fix hc0 toplevel collisions
----------------------------
revision 3.883
date: 1995/06/29 05:32:14;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/random
      template

Change regdepend rule to commit (from reg) and use likedriverlog
----------------------------
revision 3.882
date: 1995/06/29 05:28:50;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_brresp.pla, hc.V, hc_sid.Veqn: Event Daemon store sending incorrect tag to
nb when a brconflict is detected. hermesnasty_0 and standalone test
brconflictEasy noticed. Change hc_brresp to control tagen for tag7.

hc_ostate.pla: conflicting Event Daemon stores sent duplicate blocking reads
due to entering crcv mode. Changed crcv entry so that it won't be entered for
brconflict cases. Hermesnasty_0 discoveredN
```

```
Passed standalone tests: brconflictEasy (verified in ut), gauntlet
hexratio (HCDELAY=100).

placement updated.
----------------------------
revision 3.881
date: 1995/06/29 05:28:10;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/random

Build all of the regdepend tests ready for re-run
----------------------------
revision 3.880
date: 1995/06/29 01:20:24;  author: fwo;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
      vdda_partition.ly

Extend OBS4 out so that it overlaps node labels.  Required to properly
label internal vdda pads for mms.die.pad file.
----------------------------
revision 3.879
date: 1995/06/28 22:26:12;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce

fix bug in dcache_sz_16k_1
----------------------------
revision 3.878
date: 1995/06/28 22:24:16;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/xlu

avoid collisions with mc
----------------------------
revision 3.877
date: 1995/06/28 20:50:45;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

avoid collisions with lt
----------------------------
revision 3.876
date: 1995/06/28 17:00:35;  author: hopper;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      pimlib.pl


Modified all %d and %g --> %.10g n the Perl script pimlib.pl
to deal with the extended precision seen in .pim files.
----------------------------
revision 3.875
date: 1995/06/28 00:51:06;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/xlu

flat pim file pifpack off avoid toplevel collisions
----------------------------
revision 3.874
date: 1995/06/27 20:59:32;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr
```

```
avoid toplevel collisions
----------------------------
revision 3.873
date: 1995/06/27 18:34:23;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

avoid toplevel collisions
----------------------------
revision 3.872
date: 1995/06/27 17:12:25;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

make .0 release for verification
----------------------------
revision 3.871
date: 1995/06/27 08:26:59;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
      uu.V

uu/uu.V:  Multiple step algorithms that needed to to read source registers
  pairs twice as 2 sets of octlets (currently only GGFMul) injected X into
  the even/odd-distinguishing bit 0 of the later steps' Ra source register
  number.  This X is a simulation model artifact only; the real circuit
  would have worked.  Test n(a)busemul_0 noticed, although interaction with NB
  was not required.  Bug intro'd in uu.V 1.197, uu/BOM 211.0, bsrc/BOM 323.4
  from my bad single-ending thinking xor model X-sensitivity was same as mux2.
----------------------------
revision 3.870
date: 1995/06/27 01:00:15;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Make new tests available.
----------------------------
revision 3.869
date: 1995/06/27 00:07:39;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

move lt to the hole between sr/cc/es
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/BOM,v
Working file: compass/BOM
head: 7.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 67;    selected revisions: 1
description:
----------------------------
revision 4.2
date: 1995/06/29 01:19:58;  author: fwo;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
      vdda_partition.ly

Extend OBS4 out so that it overlaps node labels.  Required to properly
label internal vdda pads for mms.die.pad file.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/BOM,v
Working file: compass/layouts/BOM
head: 27.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 79;    selected revisions: 1
description:
releasebom adding BOM
----------------------------
revision 18.2
date: 1995/06/29 01:19:43;  author: fwo;  state: Exp;  lines: +2 -2
Release Target: euterpe/compass/layouts
      vdda_partition.ly

Extend OBS4 out so that it overlaps node labels.  Required to properly
label internal vdda pads for mms.die.pad file.
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/vdda_partition.ly,v
Working file: compass/layouts/vdda_partition.ly
head: 4.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 4.11
date: 1995/06/28 22:53:39;  author: chip;  state: Exp;  lines: +4 -2
periodic checkin of Wed Jun 28 15:53:06 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.cko,v
Working file: compass/layouts/vlsi.cko
head: 2.73
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 73;    selected revisions: 2
description:
----------------------------
revision 2.28
date: 1995/06/28 22:53:42;  author: chip;  state: Exp;  lines: +0 -1
periodic checkin of Wed Jun 28 15:53:06 PDT 1995
----------------------------
revision 2.27
date: 1995/06/28 22:45:18;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Wed Jun 28 15:45:17 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.log,v
```

```
Working file: compass/layouts/vlsi.log
head: 2.88
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 88;    selected revisions: 2
description:
----------------------------
revision 2.30
date: 1995/06/28 22:53:45;  author: chip;  state: Exp;  lines: +2 -0
periodic checkin of Wed Jun 28 15:53:06 PDT 1995
----------------------------
revision 2.29
date: 1995/06/28 22:45:21;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Wed Jun 28 15:45:17 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/BOM,v
Working file: doc/BOM
head: 22.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 70;    selected revisions: 2
description:
BOM for doc
----------------------------
revision 20.3
date: 1995/06/30 00:26:26;  author: jeffm;  state: Exp;  lines: +5 -1
Release Target: euterpe/doc
      testerinit.html

Initial release
----------------------------
revision 20.2
date: 1995/06/29 18:48:35;  author: doi;  state: Exp;  lines: +2 -2
Release Target: euterpe/doc
      verify.html

add description for command_test_addr to verify.html
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/testerinit.html,v
Working file: doc/testerinit.html
head: 19.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 19.1
date: 1995/06/30 00:21:16;  author: jeffm;  state: Exp;
Initial checkin of the design document for the testerinit program.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/verify.html,v
Working file: doc/verify.html
head: 18.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
----------------------------
revision 18.17
date: 1995/06/29 18:47:40;  author: doi;  state: Exp;  lines: +20 -10
rename variables Cmd_test* to Command_test*
----------------------------
revision 18.16
date: 1995/06/28 02:14:20;  author: doi;  state: Exp;  lines: +28 -2
add description of command-test-addr configuration option for hermes model
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 3
description:
----------------------------
revision 4.192
date: 1995/06/29 05:31:55;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/random
      template

Change regdepend rule to commit (from reg) and use likedriverlog
----------------------------
revision 4.191
date: 1995/06/29 05:27:52;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/random

Build all of the regdepend tests ready for re-run
----------------------------
revision 4.190
date: 1995/06/27 00:59:39;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel

Make new tests available.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makefile.cmp,v
Working file: verify/Makefile.cmp
head: 4.5
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 4.3
date: 1995/06/29 16:00:01;  author: dit00;  state: Exp;  lines: +3 -2
run hwterp step added --cerberus-node 0, --no-calliope
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makefile.rules,v
Working file: verify/Makefile.rules
head: 1.72
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 72;    selected revisions: 1
description:
----------------------------
revision 1.67
date: 1995/06/27 16:05:51;  author: lisar;  state: Exp;  lines: +21 -18
Changed waves bs inp rules
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 3
description:
----------------------------
revision 1.172
date: 1995/06/29 18:27:28;  author: jeffm;  state: Exp;  lines: +2 -2
Test that read and write alloc and no-alloc hermes commands are generated
properly.
----------------------------
revision 1.171
date: 1995/06/27 00:39:28;  author: jeffm;  state: Exp;  lines: +2 -2
Test machine checks caused by illegal cerberus responses, and by
parity errors in cerberus responses.

cerbillresp causes one machine check
carbparerr causes three machine checks

Neither test can be run on terp.
----------------------------
revision 1.170
date: 1995/06/26 20:23:23;  author: lisar;  state: Exp;  lines: +14 -2
Added setm tests, to store_unique and Makefile.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/Makefile,v
Working file: verify/perf/Makefile
head: 1.10
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/06/29 17:09:20;  author: dit00;  state: Exp;  lines: +6 -3
Added new _perf tests
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/rom_perf.S,v
Working file: verify/perf/rom_perf.S
head: 1.7
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 7;     selected revisions: 1
description:
----------------------------
revision 1.5
date: 1995/06/29 23:12:37;  author: claseman;  state: Exp;  lines: +2 -7
use cylinder 4 for more accurate count
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/BOM,v
Working file: verify/random/BOM
head: 8.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 3
description:
releasebom adding BOM
----------------------------
revision 4.1
date: 1995/06/29 05:31:45;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/random
      template

Change regdepend rule to commit (from reg) and use likedriverlog
----------------------------
revision 4.0
date: 1995/06/29 05:27:39;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/random

Build all of the regdepend tests ready for re-run
----------------------------
revision 3.1
date: 1995/06/29 05:27:33;  author: lisar;  state: Exp;  lines: +95 -29
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5557.S,v
```

```
Working file: verify/random/regdepend_r5557.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/26 15:24:47;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5757.S,v
Working file: verify/random/regdepend_r5757.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/26 15:21:48;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5957.S,v
Working file: verify/random/regdepend_r5957.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/26 15:25:55;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6152.S,v
Working file: verify/random/regdepend_r6152.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/26 15:27:29;  author: dit00;  state: Exp;
New test, ran ok
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6352.S,v
Working file: verify/random/regdepend_r6352.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/26 15:28:51;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/status,v
Working file: verify/random/status
head: 2.26
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 2.12
date: 1995/06/29 05:26:28;  author: lisar;  state: Exp;  lines: +0 -121
Empty the status file - all regdepend tests must be re-run.
Tag all of the regdepend tests that have run before.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r10803.S,v
Working file: verify/random/stgen_r10803.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/26 22:55:19;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r10987.S,v
Working file: verify/random/stgen_r10987.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
```

```
----------------------------
revision 3.1
date: 1995/06/26 14:26:56;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r11362.S,v
Working file: verify/random/stgen_r11362.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/27 22:57:45;  author: dit00;  state: Exp;
New test,ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/stgen_r11544.S,v
Working file: verify/random/stgen_r11544.S
head: 4.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 4.1
date: 1995/06/29 16:03:55;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/template,v
Working file: verify/random/template
head: 2.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 3
description:
----------------------------
revision 2.13
date: 1995/06/29 14:44:27;  author: dit00;  state: Exp;  lines: +3 -3
added latest stgen results
----------------------------
revision 2.12
date: 1995/06/29 05:31:32;  author: lisar;  state: Exp;  lines: +130 -130
Change regdepend rule to commit (from reg) and use likedriverlog
----------------------------
revision 2.11
date: 1995/06/29 05:26:30;  author: lisar;  state: Exp;  lines: +65 -66
Empty the status file - all regdepend tests must be re-run.
```

```
Tag all of the regdepend tests that have run before.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/NOTES,v
Working file: verify/standalone/hc/NOTES
head: 1.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 1.28
date: 1995/06/29 16:39:40;  author: brian;  state: Exp;  lines: +12 -0
Added woody's test for the second 'hermnasty' bug. Replaced startup.pl
with bugregress.pl.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/brconflictEasy.pl,v
Working file: verify/standalone/hc/brconflictEasy.pl
head: 10.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 10.2
date: 1995/06/28 23:00:51;  author: woody;  state: Exp;  lines: +3 -1
Modified to find verilog/bsrc/hc/BOM failure: multiple blocking reads to same
device.
----------------------------
revision 10.1
date: 1995/06/28 18:48:24;  author: woody;  state: Exp;
Add a new test, brconflictEasy that demonstrates that verilog/bsrc/hc/BOM 115.0
sends back the wrong tag on an ignored Event Daemon store.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/bugregress.pl,v
Working file: verify/standalone/hc/bugregress.pl
head: 10.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 10.2
date: 1995/06/29 16:42:41;  author: brian;  state: Exp;  lines: +2 -2
Fixed two syntax errors.
----------------------------
revision 10.1
date: 1995/06/29 16:39:42;  author: brian;  state: Exp;
Added woody's test for the second 'hermnasty' bug. Replaced startup.pl
```

```
with bugregress.pl.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/clkregress.pl,v
Working file: verify/standalone/hc/clkregress.pl
head: 7.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 7.13
date: 1995/06/29 16:39:44;  author: brian;  state: Exp;  lines: +3 -2
Added woody's test for the second 'hermnasty' bug. Replaced startup.pl
with bugregress.pl.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/hclib.pl,v
Working file: verify/standalone/hc/hclib.pl
head: 9.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 2
description:
----------------------------
revision 9.3
date: 1995/06/29 19:38:40;  author: woody;  state: Exp;  lines: +6 -1
add eclear subroutine for clearing event register.
----------------------------
revision 9.2
date: 1995/06/28 18:48:27;  author: woody;  state: Exp;  lines: +14 -3
Add a new test, brconflictEasy that demonstrates that verilog/bsrc/hc/BOM 115.0
sends back the wrong tag on an ignored Event Daemon store.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/multevnt.vec,v
Working file: verify/standalone/hc/multevnt.vec
head: 10.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 10.1
date: 1995/06/28 21:44:15;  author: brian;  state: Exp;
Added simple event test for multiple events in a row.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/nbhc_drive.V,v
Working file: verify/standalone/hc/nbhc_drive.V
head: 1.55
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 55;    selected revisions: 1
description:
----------------------------
revision 1.54
date: 1995/06/28 21:44:19;  author: brian;  state: Exp;  lines: +11 -11
Added simple event test for multiple events in a row.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/nbhcregress,v
Working file: verify/standalone/hc/nbhcregress
head: 5.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 5.14
date: 1995/06/29 16:39:45;  author: brian;  state: Exp;  lines: +1 -1
Added woody's test for the second 'hermnasty' bug. Replaced startup.pl
with bugregress.pl.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/BOM,v
Working file: verify/toplevel/BOM
head: 44.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 41.0
date: 1995/06/27 00:59:19;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/toplevel

Make new tests available.
----------------------------
revision 40.1
date: 1995/06/27 00:59:04;  author: jeffm;  state: Exp;  lines: +13 -9
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 185;   selected revisions: 3
description:
----------------------------
revision 1.172
date: 1995/06/29 18:27:28;  author: jeffm;  state: Exp;  lines: +2 -2
Test that read and write alloc and no-alloc hermes commands are generated
properly.
----------------------------
revision 1.171
date: 1995/06/27 00:39:28;  author: jeffm;  state: Exp;  lines: +2 -2
Test machine checks caused by illegal cerberus responses, and by
parity errors in cerberus responses.

cerbillresp causes one machine check
carbparerr causes three machine checks

Neither test can be run on terp.
----------------------------
revision 1.170
date: 1995/06/26 20:23:23;  author: lisar;  state: Exp;  lines: +14 -2
Added setm tests, to store_unique and Makefile.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/TODO,v
Working file: verify/toplevel/TODO
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/06/29 00:38:19;  author: jeffm;  state: Exp;
Todo list for toplevel tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cerb_registers.S,v
Working file: verify/toplevel/cerb_registers.S
head: 7.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 7.7
date: 1995/06/28 23:46:53;  author: doi;  state: Exp;  lines: +3 -3
update default values for cerb octlets 4 and 6
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cerbarbdatatest.S,v
Working file: verify/toplevel/cerbarbdatatest.S
head: 40.1
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 40.1
date: 1995/06/26 20:23:27;  author: lisar;  state: Exp;
Added setm tests, to store_unique and Makefile.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cerbillresp.S,v
Working file: verify/toplevel/cerbillresp.S
head: 40.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 40.1
date: 1995/06/27 00:39:19;  author: jeffm;  state: Exp;
Test machine checks caused by illegal cerberus responses, and by
parity errors in cerberus responses.

cerbillresp causes one machine check
carbparerr causes three machine checks

Neither test can be run on terp.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cerbparerr.S,v
Working file: verify/toplevel/cerbparerr.S
head: 40.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 40.1
date: 1995/06/27 00:39:23;  author: jeffm;  state: Exp;
Test machine checks caused by illegal cerberus responses, and by
parity errors in cerberus responses.

cerbillresp causes one machine check
carbparerr causes three machine checks

Neither test can be run on terp.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/frz_debug.sig,v
Working file: verify/toplevel/frz_debug.sig
head: 35.3
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 35.3
date: 1995/06/26 20:23:30;  author: lisar;  state: Exp;  lines: +1 -2
Added setm tests, to store_unique and Makefile.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermesnatest.S,v
Working file: verify/toplevel/hermesnatest.S
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/06/29 18:27:32;  author: jeffm;  state: Exp;
Test that read and write alloc and no-alloc hermes commands are generated
properly.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermesnatest.hconfig,v
Working file: verify/toplevel/hermesnatest.hconfig
head: 41.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 41.2
date: 1995/06/29 18:45:50;  author: jeffm;  state: Exp;  lines: +1 -1
Ooops, fixed syntax error.
----------------------------
revision 41.1
date: 1995/06/29 18:27:34;  author: jeffm;  state: Exp;
Test that read and write alloc and no-alloc hermes commands are generated
properly.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ibufhz_debug.srl,v
Working file: verify/toplevel/ibufhz_debug.srl
head: 39.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
```

```
revision 39.2
date: 1995/06/26 20:23:32;  author: lisar;  state: Exp;  lines: +2 -2
Added setm tests, to store_unique and Makefile.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/mc_debug.sig,v
Working file: verify/toplevel/mc_debug.sig
head: 40.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 40.2
date: 1995/06/26 19:08:38;  author: jeffm;  state: Exp;  lines: +20 -3
Added double machine check signals and raw machine check inputs.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/store_unique.S,v
Working file: verify/toplevel/store_unique.S
head: 7.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 7.14
date: 1995/06/26 20:23:33;  author: lisar;  state: Exp;  lines: +4 -1
Added setm tests, to store_unique and Makefile.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 2
description:
----------------------------
revision 1.109
date: 1995/06/29 16:44:28;  author: dit00;  state: Exp;  lines: +12 -1
Added new _perf tests
----------------------------
revision 1.108
date: 1995/06/26 20:23:41;  author: lisar;  state: Exp;  lines: +215 -187
Added setm tests, to store_unique and Makefile.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/vlduv_debug.sig,v
Working file: verify/toplevel/vlduv_debug.sig
head: 33.4
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 1
description:
----------------------------
revision 33.3
date: 1995/06/26 20:59:26;  author: jeffm;  state: Exp;  lines: +12 -2
Add more debugging signals.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 13
description:
top level verilog BOM
----------------------------
revision 3.655
date: 1995/06/30 02:54:07;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

latest top level placement/timing files.  950/1000
----------------------------
revision 3.654
date: 1995/06/29 18:39:59;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

fix hc0 toplevel collisions
----------------------------
revision 3.653
date: 1995/06/29 05:28:05;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_brresp.pla, hc.V, hc_sid.Veqn: Event Daemon store sending incorrect tag to
nb when a brconflict is detected. hermesnasty_0 and standalone test
brconflictEasy noticed. Change hc_brresp to control tagen for tag7.

hc_ostate.pla: conflicting Event Daemon stores sent duplicate blocking reads
due to entering crcv mode. Changed crcv entry so that it won't be entered for
brconflict cases. Hermesnasty_0 discoveredN


Passed standalone tests: brconflictEasy (verified in ut), gauntlet
hexratio (HCDELAY=100).

placement updated.
----------------------------
revision 3.652
date: 1995/06/28 22:25:52;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce
```

```
fix bug in dcache_sz_16k_1
----------------------------
revision 3.651
date: 1995/06/28 22:23:49;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/xlu

avoid collisions with mc
----------------------------
revision 3.650
date: 1995/06/28 20:50:27;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

avoid collisions with lt
----------------------------
revision 3.649
date: 1995/06/28 17:00:17;  author: hopper;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      pimlib.pl


Modified all %d and %g --> %.10g n the Perl script pimlib.pl
to deal with the extended precision seen in .pim files.
----------------------------
revision 3.648
date: 1995/06/28 00:50:41;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/xlu

flat pim file pifpack off avoid toplevel collisions
----------------------------
revision 3.647
date: 1995/06/27 20:59:12;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

avoid toplevel collisions
----------------------------
revision 3.646
date: 1995/06/27 18:34:03;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

avoid toplevel collisions
----------------------------
revision 3.645
date: 1995/06/27 17:12:03;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

make .0 release for verification
----------------------------
revision 3.644
date: 1995/06/27 08:26:40;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
      uu.V

uu/uu.V:  Multiple step algorithms that needed to to read source registers
  pairs twice as 2 sets of octlets (currently only GGFMul) injected X into
  the even/odd-distinguishing bit 0 of the later steps' Ra source register
  number.  This X is a simulation model artifact only; the real circuit
  would have worked.  Test n(a)busemul_0 noticed, although interaction with NB
```

```
  was not required.  Bug intro'd in uu.V 1.197, uu/BOM 211.0, bsrc/BOM 323.4
  from my bad single-ending thinking xor model X-sensitivity was same as mux2.
----------------------------
revision 3.643
date: 1995/06/27 00:07:16;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

move lt to the hole between sr/cc/es
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 14
description:
----------------------------
revision 325.0
date: 1995/06/30 02:53:41;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

latest top level placement/timing files.  950/1000
----------------------------
revision 324.15
date: 1995/06/30 02:53:23;  author: tbr;  state: Exp;  lines: +8 -8
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 324.14
date: 1995/06/29 18:39:34;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

fix hc0 toplevel collisions
----------------------------
revision 324.13
date: 1995/06/29 05:27:49;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_brresp.pla, hc.V, hc_sid.Veqn: Event Daemon store sending incorrect tag to
nb when a brconflict is detected. hermesnasty_0 and standalone test
brconflictEasy noticed. Change hc_brresp to control tagen for tag7.

hc_ostate.pla: conflicting Event Daemon stores sent duplicate blocking reads
due to entering crcv mode. Changed crcv entry so that it won't be entered for
brconflict cases. Hermesnasty_0 discoveredN


Passed standalone tests: brconflictEasy (verified in ut), gauntlet
hexratio (HCDELAY=100).

placement updated.
----------------------------
revision 324.12
date: 1995/06/28 22:25:35;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/ce
```

```
fix bug in dcache_sz_16k_1
----------------------------
revision 324.11
date: 1995/06/28 22:23:28;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/xlu

avoid collisions with mc
----------------------------
revision 324.10
date: 1995/06/28 20:50:11;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

avoid collisions with lt
----------------------------
revision 324.9
date: 1995/06/28 16:59:59;  author: hopper;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc
      pimlib.pl


Modified all %d and %g --> %.10g n the Perl script pimlib.pl
to deal with the extended precision seen in .pim files.
----------------------------
revision 324.8
date: 1995/06/28 00:50:15;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/xlu

flat pim file pifpack off avoid toplevel collisions
----------------------------
revision 324.7
date: 1995/06/27 20:58:53;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/sr

avoid toplevel collisions
----------------------------
revision 324.6
date: 1995/06/27 18:33:44;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

avoid toplevel collisions
----------------------------
revision 324.5
date: 1995/06/27 17:11:44;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

make .0 release for verification
----------------------------
revision 324.4
date: 1995/06/27 08:26:22;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
      uu.V

uu/uu.V:  Multiple step algorithms that needed to to read source registers
  pairs twice as 2 sets of octlets (currently only GGFMul) injected X into
  the even/odd-distinguishing bit 0 of the later steps' Ra source register
  number.  This X is a simulation model artifact only; the real circuit
```

```
  would have worked.  Test n(a)busemul_0 noticed, although interaction with NB
  was not required.  Bug intro'd in uu.V 1.197, uu/BOM 211.0, bsrc/BOM 323.4
  from my bad single-ending thinking xor model X-sensitivity was same as mux2.
----------------------------
revision 324.3
date: 1995/06/27 00:06:55;  author: dickson;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/lt

move lt to the hole between sr/cc/es
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 2
description:
----------------------------
revision 40.87
date: 1995/06/30 02:09:00;  author: tbr;  state: Exp;  lines: +27 -29
back off cycletime.  Adjust early nets
----------------------------
revision 40.86
date: 1995/06/25 05:09:23;  author: tbr;  state: Exp;  lines: +6 -7
re-instate commented out dependency in all.net generation
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
----------------------------
revision 312.5
date: 1995/06/30 02:14:16;  author: tbr;  state: Exp;  lines: +75405 -86941
latest top level data
----------------------------
revision 312.4
date: 1995/06/26 02:02:10;  author: tbr;  state: Exp;  lines: +86941 -76314
latest top level route files
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.nof,v
Working file: verilog/bsrc/chip_euterpe-base.nof
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 2
```

```
description:
----------------------------
revision 307.8
date: 1995/06/30 02:22:24;  author: tbr;  state: Exp;  lines: +51930 -51927
latest top level data
----------------------------
revision 307.7
date: 1995/06/26 02:07:49;  author: tbr;  state: Exp;  lines: +50579 -50707
latest top level route files
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 4
description:
----------------------------
revision 312.7
date: 1995/06/30 02:27:37;  author: tbr;  state: Exp;  lines: +2 -2
latest top level data
----------------------------
revision 312.6
date: 1995/06/29 17:01:20;  author: woody;  state: Exp;  lines: +1611 -1775
Fix toplevel collisions with hc0.
----------------------------
revision 312.5
date: 1995/06/27 04:46:55;  author: tbr;  state: Exp;  lines: +20 -20
save this version before moving lt
----------------------------
revision 312.4
date: 1995/06/26 02:11:01;  author: tbr;  state: Exp;  lines: +2440 -2517
latest top level route files
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.strength,v
Working file: verilog/bsrc/chip_euterpe-base.strength
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 2
description:
----------------------------
revision 312.5
date: 1995/06/30 02:29:46;  author: tbr;  state: Exp;  lines: +50008 -58111
latest top level data
----------------------------
revision 312.4
date: 1995/06/26 02:12:20;  author: tbr;  state: Exp;  lines: +58111 -50004
latest top level route files
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.xrf,v
Working file: verilog/bsrc/chip_euterpe-base.xrf
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 2
description:
----------------------------
revision 307.8
date: 1995/06/30 02:33:15;  author: tbr;  state: Exp;  lines: +32803 -32866
latest top level data
----------------------------
revision 307.7
date: 1995/06/26 02:15:22;  author: tbr;  state: Exp;  lines: +25199 -25208
latest top level route files
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/pimlib.pl,v
Working file: verilog/bsrc/pimlib.pl
head: 37.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 37.8
date: 1995/06/28 15:27:30;  author: hopper;  state: Exp;  lines: +11 -11
Modified all %d and %g --> %.10g to deal with the extended precision
seen in .pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/BOM,v
Working file: verilog/bsrc/ce/BOM
head: 86.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 170;   selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 82.0
date: 1995/06/28 22:25:17;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/ce

fix bug in dcache_sz_16k_1
----------------------------
revision 81.1
date: 1995/06/28 22:25:08;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/ce/ce_mck.V,v
Working file: verilog/bsrc/ce/ce_mck.V
head: 32.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 32.13
date: 1995/06/28 17:21:48;  author: dickson;  state: Exp;  lines: +3 -1
fix bug in dcache_sz_16k_1
no placement change required.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 117.0
date: 1995/06/29 18:39:11;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

fix hc0 toplevel collisions
----------------------------
revision 116.1
date: 1995/06/29 18:39:03;  author: woody;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 116.0
date: 1995/06/29 05:27:33;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

hc_brresp.pla, hc.V, hc_sid.Veqn: Event Daemon store sending incorrect tag to
nb when a brconflict is detected. hermesnasty_0 and standalone test
brconflictEasy noticed. Change hc_brresp to control tagen for tag7.

hc_ostate.pla: conflicting Event Daemon stores sent duplicate blocking reads
due to entering crcv mode. Changed crcv entry so that it won't be entered for
brconflict cases. Hermesnasty_0 discoveredN


Passed standalone tests: brconflictEasy (verified in ut), gauntlet
hexratio (HCDELAY=100).

placement updated.
----------------------------
revision 115.1
date: 1995/06/29 05:27:26;  author: woody;  state: Exp;  lines: +7 -7
```

```
releasebom: File needs to be up-to-date to use commit -r
===================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc.V,v
Working file: verilog/bsrc/hc/hc.V
head: 1.56
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 56;    selected revisions: 1
description:
----------------------------
revision 1.55
date: 1995/06/29 00:34:42;  author: woody;  state: Exp;  lines: +6 -5
hc_brresp.pla, hc.V, hc_sid.Veqn: Event Daemon store sending incorrect tag to
nb when a brconflict is detected. hermesnasty_0 and standalone test
brconflictEasy noticed. Change hc_brresp to control tagen for tag7.

hc_ostate.pla: conflicting Event Daemon stores sent duplicate blocking reads
due to entering crcv mode. Changed crcv entry so that it won't be entered for
brconflict cases. Hermesnasty_0 discoveredN


Passed standalone tests: brconflictEasy (verified in ut), gauntlet
hexratio (HCDELAY=100).

placement to follow
===================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0.power.tab.top,v
Working file: verilog/bsrc/hc/hc0.power.tab.top
head: 68.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 68.8
date: 1995/06/29 17:06:43;  author: tbr;  state: Exp;  lines: +961 -3232
update from latest top level
===================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0_control.pim,v
Working file: verilog/bsrc/hc/hc0_control.pim
head: 73.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;    selected revisions: 2
description:
----------------------------
revision 73.22
date: 1995/06/29 18:37:58;  author: woody;  state: Exp;  lines: +5 -5
```

```
fix toplevel collisions
----------------------------
revision 73.21
date: 1995/06/29 05:26:14;  author: woody;  state: Exp;  lines: +8 -6
Update placement.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc1_control.pim,v
Working file: verilog/bsrc/hc/hc1_control.pim
head: 73.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 73.13
date: 1995/06/29 05:26:16;  author: woody;  state: Exp;  lines: +4 -2
Update placement.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_brresp.pla,v
Working file: verilog/bsrc/hc/hc_brresp.pla
head: 65.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 65.3
date: 1995/06/29 00:34:47;  author: woody;  state: Exp;  lines: +15 -11
hc_brresp.pla, hc.V, hc_sid.Veqn: Event Daemon store sending incorrect tag to
nb when a brconflict is detected. hermesnasty_0 and standalone test
brconflictEasy noticed. Change hc_brresp to control tagen for tag7.

hc_ostate.pla: conflicting Event Daemon stores sent duplicate blocking reads
due to entering crcv mode. Changed crcv entry so that it won't be entered for
brconflict cases. Hermesnasty_0 discoveredN


Passed standalone tests: brconflictEasy (verified in ut), gauntlet
hexratio (HCDELAY=100).

placement to follow
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_ostate.pla,v
Working file: verilog/bsrc/hc/hc_ostate.pla
head: 3.26
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
```

```
description:
----------------------------
revision 3.26
date: 1995/06/29 00:34:51;  author: woody;  state: Exp;  lines: +3 -2
hc_brresp.pla, hc.V, hc_sid.Veqn: Event Daemon store sending incorrect tag to
nb when a brconflict is detected. hermesnasty_0 and standalone test
brconflictEasy noticed. Change hc_brresp to control tagen for tag7.

hc_ostate.pla: conflicting Event Daemon stores sent duplicate blocking reads
due to entering crcv mode. Changed crcv entry so that it won't be entered for
brconflict cases. Hermesnasty_0 discoveredN


Passed standalone tests: brconflictEasy (verified in ut), gauntlet
hexratio (HCDELAY=100).

placement to follow
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_sid.Veqn,v
Working file: verilog/bsrc/hc/hc_sid.Veqn
head: 3.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 3.13
date: 1995/06/29 00:34:55;  author: woody;  state: Exp;  lines: +5 -3
hc_brresp.pla, hc.V, hc_sid.Veqn: Event Daemon store sending incorrect tag to
nb when a brconflict is detected. hermesnasty_0 and standalone test
brconflictEasy noticed. Change hc_brresp to control tagen for tag7.

hc_ostate.pla: conflicting Event Daemon stores sent duplicate blocking reads
due to entering crcv mode. Changed crcv entry so that it won't be entered for
brconflict cases. Hermesnasty_0 discoveredN


Passed standalone tests: brconflictEasy (verified in ut), gauntlet
hexratio (HCDELAY=100).

placement to follow
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/BOM,v
Working file: verilog/bsrc/lt/BOM
head: 98.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 196;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
```

```
revision 97.0
date: 1995/06/27 18:33:18;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/lt

avoid toplevel collisions
----------------------------
revision 96.1
date: 1995/06/27 18:33:10;  author: dickson;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 96.0
date: 1995/06/27 00:06:33;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/lt

move lt to the hole between sr/cc/es
----------------------------
revision 95.1
date: 1995/06/27 00:06:24;  author: dickson;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/genpim.pl,v
Working file: verilog/bsrc/lt/genpim.pl
head: 56.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 2
description:
----------------------------
revision 56.6
date: 1995/06/27 18:32:09;  author: dickson;  state: Exp;  lines: +1 -3
avoid toplevel collisions
----------------------------
revision 56.5
date: 1995/06/27 00:04:47;  author: dickson;  state: Exp;  lines: +5 -5
moved lt to the hole between sr/cc/es.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/lt_control.pim,v
Working file: verilog/bsrc/lt/lt_control.pim
head: 56.19
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 19;    selected revisions: 2
description:
----------------------------
revision 56.19
date: 1995/06/27 18:32:11;  author: dickson;  state: Exp;  lines: +278 -362
avoid toplevel collisions
----------------------------
revision 56.18
date: 1995/06/27 00:04:50;  author: dickson;  state: Exp;  lines: +3 -3
moved lt to the hole between sr/cc/es.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/lt/pimlib.pl,v
Working file: verilog/bsrc/lt/pimlib.pl
head: 56.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 56.14
date: 1995/06/27 18:32:13;  author: dickson;  state: Exp;  lines: +1 -109
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/BOM,v
Working file: verilog/bsrc/sr/BOM
head: 75.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 73.0
date: 1995/06/28 20:49:54;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/sr

avoid collisions with lt
----------------------------
revision 72.1
date: 1995/06/28 20:49:47;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 72.0
date: 1995/06/27 20:58:36;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/sr

avoid toplevel collisions
----------------------------
revision 71.1
date: 1995/06/27 20:58:28;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/sr/sr.pim,v
Working file: verilog/bsrc/sr/sr.pim
head: 51.12
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 12;    selected revisions: 2
```

```
description:
----------------------------
revision 51.12
date: 1995/06/28 20:49:08;  author: dickson;  state: Exp;  lines: +2 -2
avoid collisions with lt
----------------------------
revision 51.11
date: 1995/06/27 20:57:43;  author: dickson;  state: Exp;  lines: +3 -3
avoid toplevel collisions
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 2
description:
----------------------------
revision 212.0
date: 1995/06/27 17:11:25;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu

make .0 release for verification
----------------------------
revision 211.1
date: 1995/06/27 08:26:02;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu
      uu.V

uu/uu.V:  Multiple step algorithms that needed to to read source registers
  pairs twice as 2 sets of octlets (currently only GGFMul) injected X into
  the even/odd-distinguishing bit 0 of the later steps' Ra source register
  number.  This X is a simulation model artifact only; the real circuit
  would have worked.  Test n(a)busemul_0 noticed, although interaction with NB
  was not required.  Bug intro'd in uu.V 1.197, uu/BOM 211.0, bsrc/BOM 323.4
  from my bad single-ending thinking xor model X-sensitivity was same as mux2.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v
Working file: verilog/bsrc/uu/uu.V
head: 1.202
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 202;   selected revisions: 1
description:
issue unit
----------------------------
revision 1.198
date: 1995/06/27 08:25:18;  author: mws;  state: Exp;  lines: +3 -3
Multiple step algorithms that needed to to read source registers
  pairs twice as 2 sets of octlets (currently only GGFMul) injected X into
  the even/odd-distinguishing bit 0 of the later steps' Ra source register
```

```
  number.  This X is a simulation model artifact only; the real circuit
  would have worked.  Test n(a)busemul_0 noticed, although interaction with NB
  was not required.  Bug intro'd in uu.V 1.197
  from my bad single-ending thinking xor model X-sensitivity was same as mux2.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/BOM,v
Working file: verilog/bsrc/xlu/BOM
head: 65.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 6
description:
releasebom adding BOM
----------------------------
revision 65.0
date: 1995/06/30 02:52:19;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

latest top level placement/timing files.  950/1000
----------------------------
revision 64.1
date: 1995/06/30 02:52:11;  author: tbr;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 64.0
date: 1995/06/28 22:23:04;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/xlu

avoid collisions with mc
----------------------------
revision 63.1
date: 1995/06/28 22:22:56;  author: dickson;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 63.0
date: 1995/06/28 00:49:51;  author: dickson;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/xlu

flat pim file pifpack off avoid toplevel collisions
----------------------------
revision 62.1
date: 1995/06/28 00:49:42;  author: dickson;  state: Exp;  lines: +5 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/Makefile,v
Working file: verilog/bsrc/xlu/Makefile
head: 1.48
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 48;    selected revisions: 2
description:
```

```
----------------------------
revision 1.48
date: 1995/06/29 04:59:31;  author: tbr;  state: Exp;  lines: +4 -17
correct pim dependencies for new flat file
----------------------------
revision 1.47
date: 1995/06/28 00:48:27;  author: dickson;  state: Exp;  lines: +6 -1
in fixing collisions at top level i resorted to turning
pifpack off in non-custom areas and started using a flat
pim file (snapshot of tbr's xlu-base.pim file)
other wise i couldn't predict what collision would happen
next time around after attempting to fix the two cells
that didn't place for chip_euterpe-iter currently in tbr's area.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/genpim.pl,v
Working file: verilog/bsrc/xlu/genpim.pl
head: 8.21
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 21;    selected revisions: 1
description:
----------------------------
revision 8.21
date: 1995/06/28 00:48:31;  author: dickson;  state: Exp;  lines: +12 -31
in fixing collisions at top level i resorted to turning
pifpack off in non-custom areas and started using a flat
pim file (snapshot of tbr's xlu-base.pim file)
other wise i couldn't predict what collision would happen
next time around after attempting to fix the two cells
that didn't place for chip_euterpe-iter currently in tbr's area.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/pimlib.pl,v
Working file: verilog/bsrc/xlu/pimlib.pl
head: 8.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 8.20
date: 1995/06/28 00:48:34;  author: dickson;  state: Exp;  lines: +7 -532
in fixing collisions at top level i resorted to turning
pifpack off in non-custom areas and started using a flat
pim file (snapshot of tbr's xlu-base.pim file)
other wise i couldn't predict what collision would happen
next time around after attempting to fix the two cells
that didn't place for chip_euterpe-iter currently in tbr's area.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/xlu/xlu.pim,v
Working file: verilog/bsrc/xlu/xlu.pim
```

```
head: 62.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 2
description:
----------------------------
revision 62.2
date: 1995/06/28 22:21:53;  author: dickson;  state: Exp;  lines: +2 -2
avoid collisions with mc
----------------------------
revision 62.1
date: 1995/06/28 00:44:39;  author: dickson;  state: Exp;
flat pim file taken from xlu-base.pim in tbrs area.
xlu was pifpacking the non custom areas of the layout
making it impossible (or at least a crap shoot)
to determine where cells would finally land
when included in the top level placement of euterpe.
parts along outer edges move at all stages of gards
flow at the individual block level.
=============================================================================
```